## Tiling based FPGA Acceleration for 3D CT Reconstruction

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Figure: Figure 1a: A demonstration of the tiling. Different colors represent different tiles. Our tiles are of the shape (x, y, z); Figure 1b: A block of the measured projection data and its related tiles. Solid red lines represent a group of X-ray beams and the blue tiles are its in-use cache.

Find out the best (x, y, z) options to minimize the amount of memory I/O F(x, y, z, g) given a sequence of projection g with the constraint of maximum BRAM size.

Data reuse rate = 
$$\frac{N_x \cdot N_y \cdot L}{F(x, y, z, g)}$$
, (1)

